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TITLE OF THE INVENTION:	Enhanced Automatic Gain Control Mechanism for the UE in Time Slotted Data Transmissions

INSTRUCTIONS

All questions must be answered before the Disclosure can be processed. Attach separate pages when necessary. Sign and date each page and any additional pages in ink using your full legal name. Please have two witnesses sign and date every page including supplements to the Invention Disclosure. A co-inventor cannot be a witness.

QUESTIONS BELOW MUST BE ANSWERED: (Attach separate pages when necessary)

The field of technology the Invention relates to: ☒ Layer 1 ☐ Layer 2 ☐ Layer 3

☐ 802.____ ☐ Other ____ ☒ TDD ☐ FDD ☒ TDSCDMA ☐ OFDM

☐ ARIB ☒ UMTS ☒ CDMA ☐ CDMA 2000

Please classify your Invention as: ____ System ____ Chip ____ UE

Will this be submitted to a standards body? If so, please identify the form number and date of submission – and attach a copy (or insert hyperlink): ____

When did you first begin to work on the invention? ____

Did any work concerning the invention arise in the course of any contract? ☐YES ☐ NO; if yes, identify:____

Is further development of your invention now in progress or scheduled? ☐YES ☐ NO

Are there any plans to publish or otherwise disseminate any aspect of this invention in the future? ☐YES ☐NO; if yes, please identify and list dates. ____

READ AND UNDERSTOOD BY:	
Inventor (1):	Witness #1
Inventor (2)	Witness #2
Date:	Date:

Description of the invention

Describe your invention in specific detail so that a person who is technically competent, but who may not be familiar with your line of work will be able to understand it. You must give sufficient information to allow someone to make and use the invention without undue experimentation. The description should include the following:

a. The background of the state of technology existing before your invention: This patent is an enhancement to another patent already submitted as a patent disclosure, the name of which was: Automatic Gain Control Mechanism for the UE in Time Slotted Data Transmissions

b. The problem solved by the invention: Saturation causes the AGC to behave poorly in cases where the incoming signal power level significantly changes from slot to slot

c. The advantages of your invention over the prior work: The invention proposes a method to improve performance in these conditions

d. Drawings illustrating/describing your invention: See attachment

e. Whether the part, (or its form or interconnection) is *ESSENTIAL* to the invention. For example, ask yourself, "If this part were left out, or changed, would the remaining device still be my invention?" Or, "If this part were changed or left out, would the invention still work? This may include any critical limitations such as angle, temperature, size, etc. _____

f. Provide labeled sketches to detail your invention. Be sure all essential parts are shown on the sketch, and try not to include extraneous details. Measurements are not required, unless they are essential to the operation of the invention. _____

Prior Art

Attach a copy and citation of all publications, patents, etc. which are known to you, which relate to your invention, and which would be important to consider in understanding how your invention differs from prior work.

Alternatives

You have described the best way to build (perform) your invention. Now consider the alternatives. Is there any other way to perform your invention? _____If so, how? _____

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If you have any questions regarding this disclosure please contact:

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1.1 (this is a temporary heading used as a placeholder to satisfy the automatic cross referencing of figures, equations, and section headings – remove before flight)

1.1.1.1 UE AGC

1.1.1.1.1 Introduction

This section provides a description of the **steady state TDD UE** AGC algorithm proposed for L1 implementation.

1.1.1.1.2 High Level Description

The UE AGC design presented in this document uses fixed-point settings derived from the basic assumption that the ADC word size is 8 bits (7 magnitude, 1 sign bit).

It is also assumed that

- The cell search process has completed successfully and the slot timing has been acquired.
- The cell search AGC provides an initial value.
- The total gain of the RF chain has been applied to the received signal and is reflected in the values of the signal at the input of the digital controlled gain block.
- The RF chain is designed to provide a specified signal level at the ADC input, for unity gain setting.

The steady state UE AGC algorithm is slot based. For each time slot, the following three steps are taken.

1. Initialize the digital controlled gain before each slot arrives. This step is called the *Initialization Process*.
2. Adjust the digital controlled gain, for a specified number of iterations, so that the power at the output of ADC is close to a reference power level. This step is the*the AGC on period.*
3. After the closed-loop process, the loop is opened. The gain computed at the end of the closed-loop process is then used for the rest of the time slot. This step is the*AGC off period.*

1.1.1.1.2.1 Top-Level Block Diagram

A top-level block diagram of the AGC is shown in Figure 1.1.3. The original AGC from TVP is shown as the AGC Loop block in this diagram. The Saturation Detect, Erase, and DC Cancel blocks are new blocks. The RRC Filter block is not part of AGC but is included here to show where the other blocks fit relative to it. (Note: The acronym AGC henceforth refers to the original function plus enhancements and the original inner loop process is now referred to as the AGC Loop.)

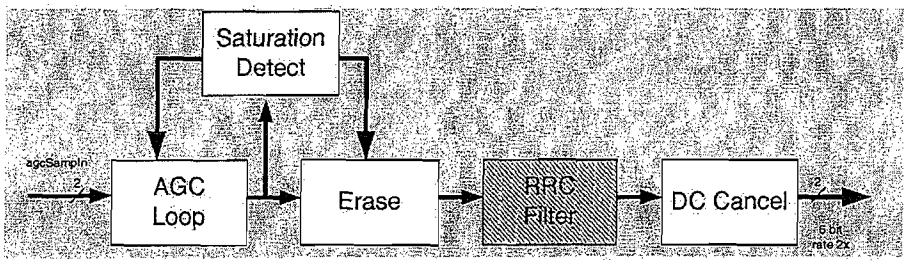

Figure 1.1.3 Top-level block diagram of AGC

1.1.1.1.3 AGC Algorithm Description

The block diagram of the enhanced AGC process is shown in Figure 1.1.4. In addition to the closed loop processing, it illustrates the manner in which the saturation detection function provides additional power corrections into the loop for the more extreme cases of signal saturation. It also illustrates the condition under which the Erase function is activated for a given block: the condition is satisfied when the saturation count exceeds the threshold ζ. Two gain initialization options are indicated, one that employs the final calculated gain from the previous frame for the current slot together with a correction factor Δ, and the other which uses a pre-set constant gain for all slots over all time. Once the AGC is in steady state, the accumulator block receives inputs, once per iteration, from the Power Comparator block only.

Figure 1.1.4 also depicts the positions in the data flow of the bit selector (low, middle, or high six bits) and the equalization function.

Each of these functions is described in detail below.

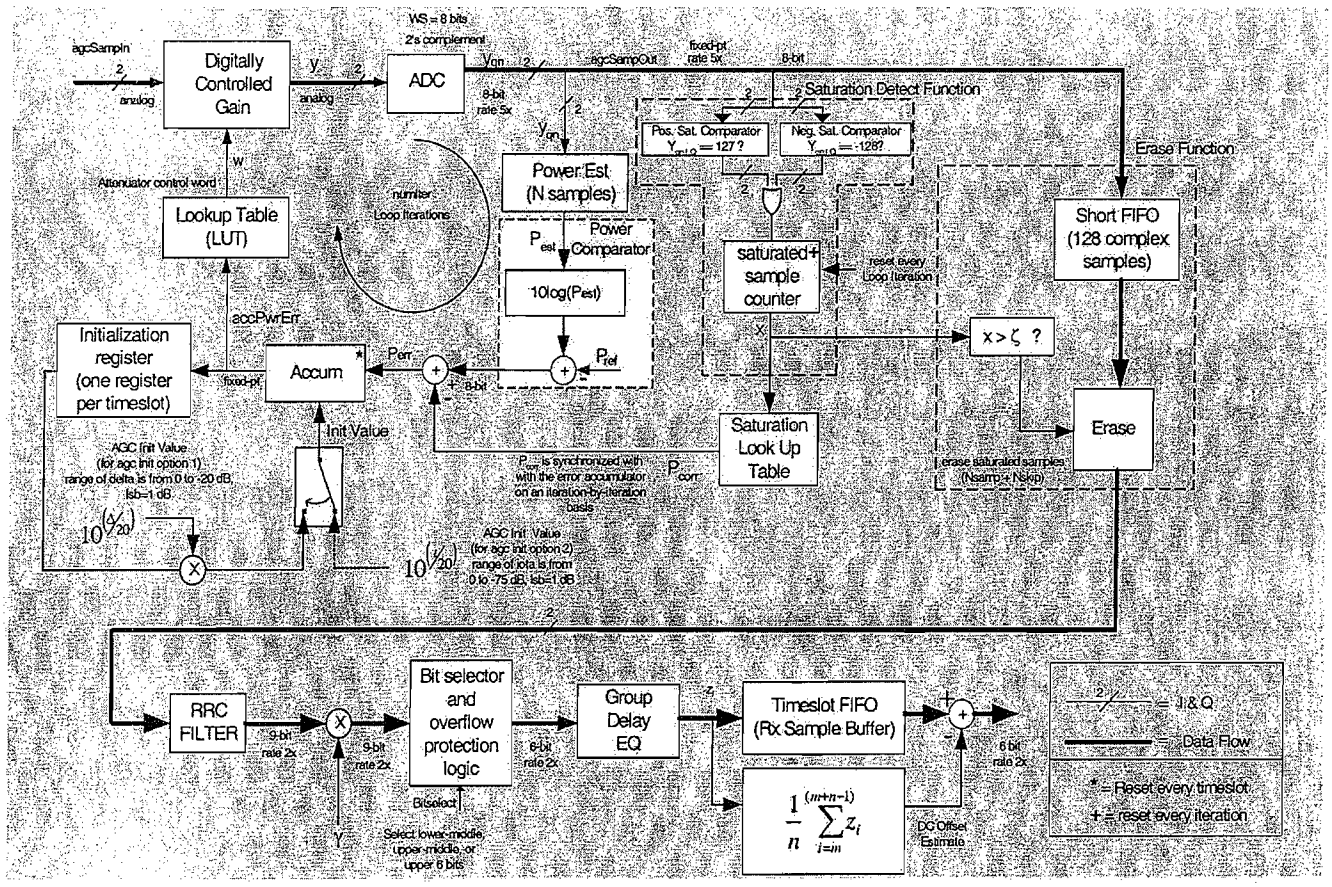

Figure 1.1.4. Block Diagram of AGC

1.1.1.1.3.1 AGC Slot Processing

The flow chart for AGC processing during a slot is shown in Figure 1.1.6.

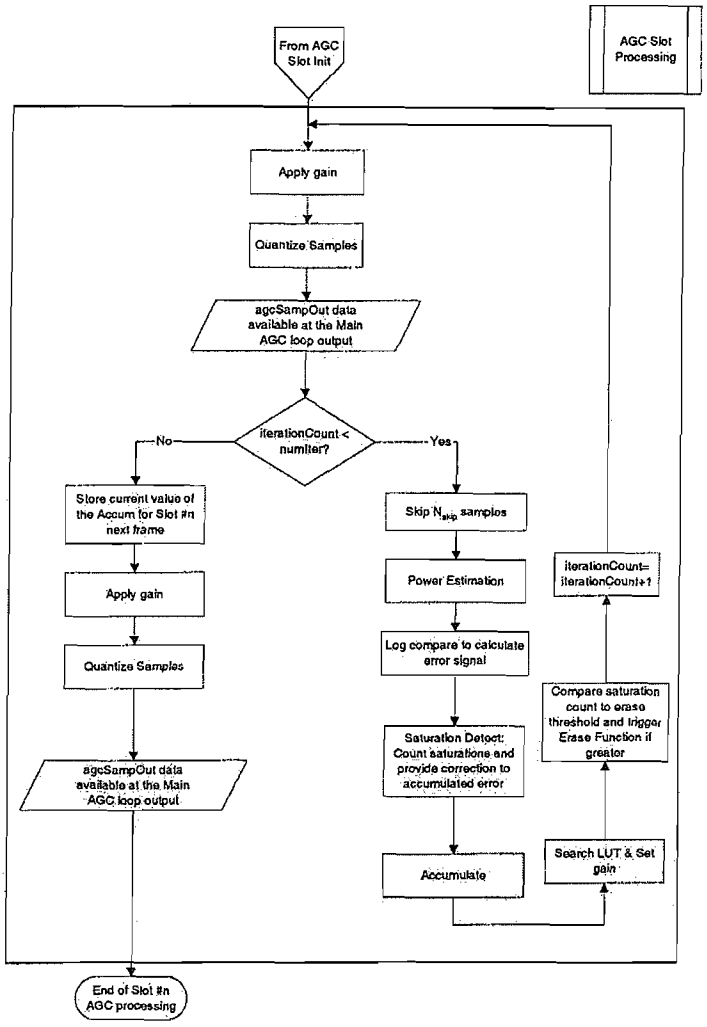

Figure 1.1.6. Flow chart for AGC slot processing

From the above figures we see that, in any given active slot of a frame, the following operations occur over the time slot:

First, initialize the accumulator and the digital controlled gain setting. For the current gain setting, the ADC samples the received signal at 5x sampling rate (i.e. 5 times the chip rate). The quantized samples y_{qn} (for the I and Q channels) are fed to the power estimation block, which estimates the power at the ADC output, using a number of N_{samp} samples. Provisions should be made to allow the power estimation block to skip the first N_{skip} samples immediately following the update of the gain. This is to prevent transients due to gain setting latency from impacting the power estimation. The estimated power is compared to the desired reference level, using a log comparator (power comparator). The error signal at the output of the comparator is accumulated into the accumulator block. The output of the accumulator is used to drive a lookup table (LUT) which provides the control word for the digitally controlled gain for the next iteration. After a few iterations, the control word is frozen and kept in a buffer for the same time slot in the next frame. The digitally controlled gain is set using this control word for the rest of time slot.

1.1.1.1.3.2 Inputs

1.1.1.1.3.2.1 Data

- sampIn = analog baseband signals (continuous time) for the I and Q channels

1.1.1.1.3.2.2 Control

- Slot timing information – this is needed to ensure the following:
  - Correct initialization of the accumulator bank and digital controlled gain setting at the beginning of the slot
  - Correct alignment of the power measurement block at slot boundaries
- ADC sampling clock signal – this is needed to provide the desired sampling rate of 5x, i.e. 5 x 3.84 MHz = 19.2 MHz.

1.1.1.1.3.3 Outputs

1.1.1.1.3.3.1 Data

- digital samples for the I & Q channels, sampled at 2x and quantized to 6 bits

1.1.1.1.3.3.2 Control

- None

1.1.1.1.3.4 Frequency of Operation

The AGC operates each active Rx slot.

1.1.1.1.3.5 Parameters

The AGC can be configured with the parameters described in Table 1.1.1 below.

Table 1.1.1. Configurable parameters for AGC

Parameter	Identifier	Unit	Default	Min	Max	LSB	Notes
Reference level	P_{ref}	dB	24	21	33	1	Note 1
Number of loop iterations	numIter	integer	3	2	4	1	Note 3
Power Estimation Wait Time	N_{skip}	Chips	14	0	16	1	Note 2
		Samples	70	0	80	5x#of chips	
Number of samples used in the power estimation block	N_{chips}	Chips	16	[8]	[64]	1	Note 3
	N_{samp}	samples	80	[40]	[320]	5x# of chips	
Initial Gain	i	dB	0	-75	0	1	Used only for agc init option 1 Note 4
AGC initialization gain offset	Δ	dB	-15	-40	0	1	Used only for agc init option 2
Eraser threshold	ζ	integer	[ ]	0	[400]	0.0625	
Fine gain adjustment	γ	gain	1.0	0.5	1.0		
Bit selection	Bitselect	integer	2	1	3	1	
Saturation compensation enable	Satcomp_enable	integer	1	0	1	NA	1=enable 0=disable
EQ enable	EQ_enable	integer	1	0	1	NA	1=enable 0=disable
DC offset compensation enable	DCoffset_enable	integer	1	0	1	NA	1=enable 0=disable
Eraser enable	Eraser_enable	integer	1	0	1	NA	1=enable 0=disable
Init Select	Init_select	Integer		0	1	NA	0=option 1 1=option 2

Notes

1. The reference level P_{ref} is calculated by requiring output data for I or Q channel to satisfy

   $P(-2^5 < Y < 2^5) = [\ ]\%$ (on the order of 95 to 99%)

   and assuming the input data on I and Q are independent Gaussian variables.

2. The power estimation block should be configured to skip the first N_{skip} chips immediately following the update of the gain. This is to prevent transients due to gain setting latency from impacting the power estimation. The maximum value for N_{skip} shall not exceed the gain setting delay that is hardware dependent.
3. The value for the "Number of samples used in the power estimation block" does not include the number of samples to skip prior to power estimation. In addition, the values of number of loop iterations presented in Table 1.1.1 assume that the power estimation is performed for 16 chips. The number of loop iterations may be increased if the power estimation block uses less than 16 chips for power measurement. For example, if the power estimation block uses 8 chips for power measurement, then the number of loop iterations may be increased to 6.
4. The number shown in this row is the gain value above the minimum gain, G_{init}-G_{min}. It is selected based on the criterion that if the power of the input signal is at its maximum value, this gain will not saturate the ADC.

1.1.1.1.3.6 Performance Requirements

- Convergence: the AGC Loop must converge in [3*30] chips or less. (TVP values subject to change.)
- Error Margin: The error margin for the AGC Loop convergence can be estimated as follows. If the ADC size is 8 bits (i.e. 1 sign bit and 7 magnitude bits) and the desired power level at the ADC input corresponds to 4 magnitude bits, then there is a margin of 3 magnitude bits, that is 3 x 6 dB = 18 dB margin. Allowing 9 dB of headroom for signal peak to average ratio or channel variation, it follows that the bias and the standard deviation of the gain setting must satisfy the following relation:

$$bias + 2 \cdot std \leq 9\ dB$$

1.1.1.1.4 Detailed Description

This section describes each of the AGC blocks.

1.1.1.1.4.1 Initialization

The flowchart for the initialization process before each active slot arrives is shown in Figure 1.1.7.

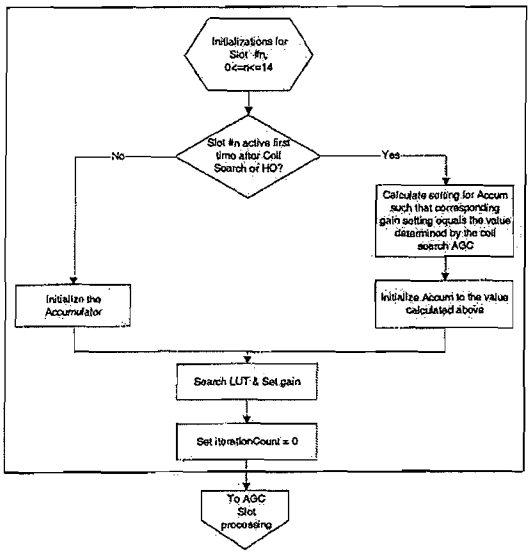

Figure 1.1.7. Flowchart for Initialization

Note that in the left branch of the initialization flow chart, the implementation of the AGC initialization process should allow selecting one of two initialization options. The two initialization options are:

Option 1: Using the accumulated error at the end of the closed-loop process of this slot in the previous frame, plus an offset, denoted Δ, in dB. The range for Δ is from 0 to [–20] dB in 1 dB steps, and it is stored in persistent memory (e.g. FLASH ROM) as a fixed configuration parameter. The range specified is consistent with the input exponential shown in Figure 1.1.4, which expect a value in dB.

Option 2: Using a pre-set initial constant value, denoted ι, in dB. The range for ι is from 0 to [–75] dB in 1 dB steps, and it is stored in persistent memory (e.g. FLASH ROM) as a fixed configuration parameter. The range specified is consistent with the input exponential shown in Figure 1.1.4, which expect a value in dB.

The initialization option 1 versus option 2 is controlled via the configuration parameter Init_select.

1.1.1.1.4.2 Digitally Controlled Gain

The gain range is 0 to 75 dB, with steps of 1 dB. Therefore, the signal gain can be expressed as $10^{w/20}$, where w is the control word.

1.1.1.1.4.3 ADC

The recommended ADC word size is 8 bits, 2's complement representation.

1.1.1.1.4.4 Power Estimation Block

1.1.1.1.4.4.1 Inputs

y_{qn} = Quantized complex samples (i.e. I and Q channels) at the ADC output, sampled at 5x

1.1.1.1.4.4.2 Outputs

P_{est} = estimated power, calculated as:

$$P_{est} = \frac{1}{N_{samp}} \cdot \sum_{n=1}^{N_{samp}} \left| y_{qn} \right|^2 \qquad (1.1.1.1.1)$$

where: N_{samp} is the number of samples used for power estimation (see Table 1.1.1), default value $N_{samp} = 80$.

Note that the P_{est} is the power estimate at the ADC output, so if the ADC is saturated, then P_{est} does not estimate correctly the power at the ADC input.

1.1.1.1.4.4.3 Fixed point settings

This section presents the fixed-point settings for the power estimation block.

Table 1.1.3. Fixed point settings for the power estimation block

	Word Size WS (bits)	Number of Fractional Bits
y_{qn}	8	0
$\lvert y_{qn} \rvert^2$	17	0
accumulator	24 (see note)	0
P_{est}	24	0

Note

The implementation of the AGC Loop runs at 5x sampling rate, $N_{samp} = 80$ add operations are needed. This means that the accumulator size must be $17 + \log_2(80) = 17 + 6.32 = 24$ bits to prevent overflows.

Alternately, to alleviate the need for scaling with the $1/N_{samp}$ factor, the power estimation block may calculate $P_1 = \sum_{n=1}^{N_{samp}} \lvert y_{qn} \rvert^2$, in which case the input of the power comparator block needs to be scaled accordingly: $N_{samp} \cdot P_{ref}$.

1.1.1.1.4.5 Power Comparator Block

This block is used during the closed-loop process, as well as at the end of open loop process.

1.1.1.1.4.5.1 Inputs

- P_{est} = power estimate (see Section 1.1.1.1.4.4)
- P_{ref} = reference power. The value of the reference power needs to be calculated such that the AGC Loop provides an average power level at the input of the ADC that corresponds to 4 magnitude bits.

1.1.1.1.4.5.2 Outputs

- pwrErr = error signal measuring the power setting error. It is calculated as follows:

$$pwrErr = 10 \cdot \log_{10}\left(\frac{P_{ref}}{P_{est}}\right) \qquad \textbf{(1.1.1.1.2)}$$

1.1.1.1.4.6 Power Error Calculation

This block is used during the closed-loop process, as well as at the end of open loop process. It adjusts the power error $pwrErr$ by an amount P_{corr} which depends on the saturation level.

1.1.1.1.4.6.1 Inputs

- P_{corr} = power correction from Saturation LUT
- pwrErr = see section 1.1.1.1.4.5.2.

1.1.1.1.4.6.2 Outputs

- P_{err} = error signal which includes saturation level adjustment. It is calculated as follows:

$$P_{err} = pwrErr - P_{corr}$$

1.1.1.1.4.7 Error Signal Accumulator

The operation of the AGC Loop requires storage of the accumulator values at the end of each slot. A memory area of 15 words is therefore required. This block is used during the closed-loop process, as well as at the end of open loop process.

1.1.1.1.4.7.1 Input

- Perr = error signal—see section 1.1.1.1.4.6.2.

1.1.1.1.4.7.2 Output

- accPwrErr = accumulated error signal.

1.1.1.1.4.8 Lookup Table (LUT)

1.1.1.1.4.8.1 Operation

The LUT shall be designed to provide the gain control word that corresponds to the desired gain settings in steps of 1 dB for a total range of 0 to 75 dB, as per the current IDC RF design.

1.1.1.1.4.8.2 Input

- accPwrErr = accumulated error signal from the accumulator output

1.1.1.1.4.8.3 Output

- w = gain control word to achieve the desired gain setting

1.1.1.1.4.9 Saturation Detect

In order to compensate for under-valued power estimates due to large saturation counts, the Saturation Detect algorithm is introduced. It consists of two parts:

- Saturated Sample Counter
- Positive and negative saturation comparators

1.1.1.1.4.9.1 Operation

Saturation Detect is started by counting the number of samples output from the signed 8-bit ADC that have values -128 or +127. The count is performed every Nsamp period following an Nskip period and it is reset each iteration. The ratio of saturated samples to the number of samples in an Nsamp period is used to form the estimate of the amount of saturation. If either the I or Q parts of a given input value is –128 or +127, the saturation counter is incremented. The resulting count at the end of an Nsamp period is used as an input to the Saturation Lookup Table.

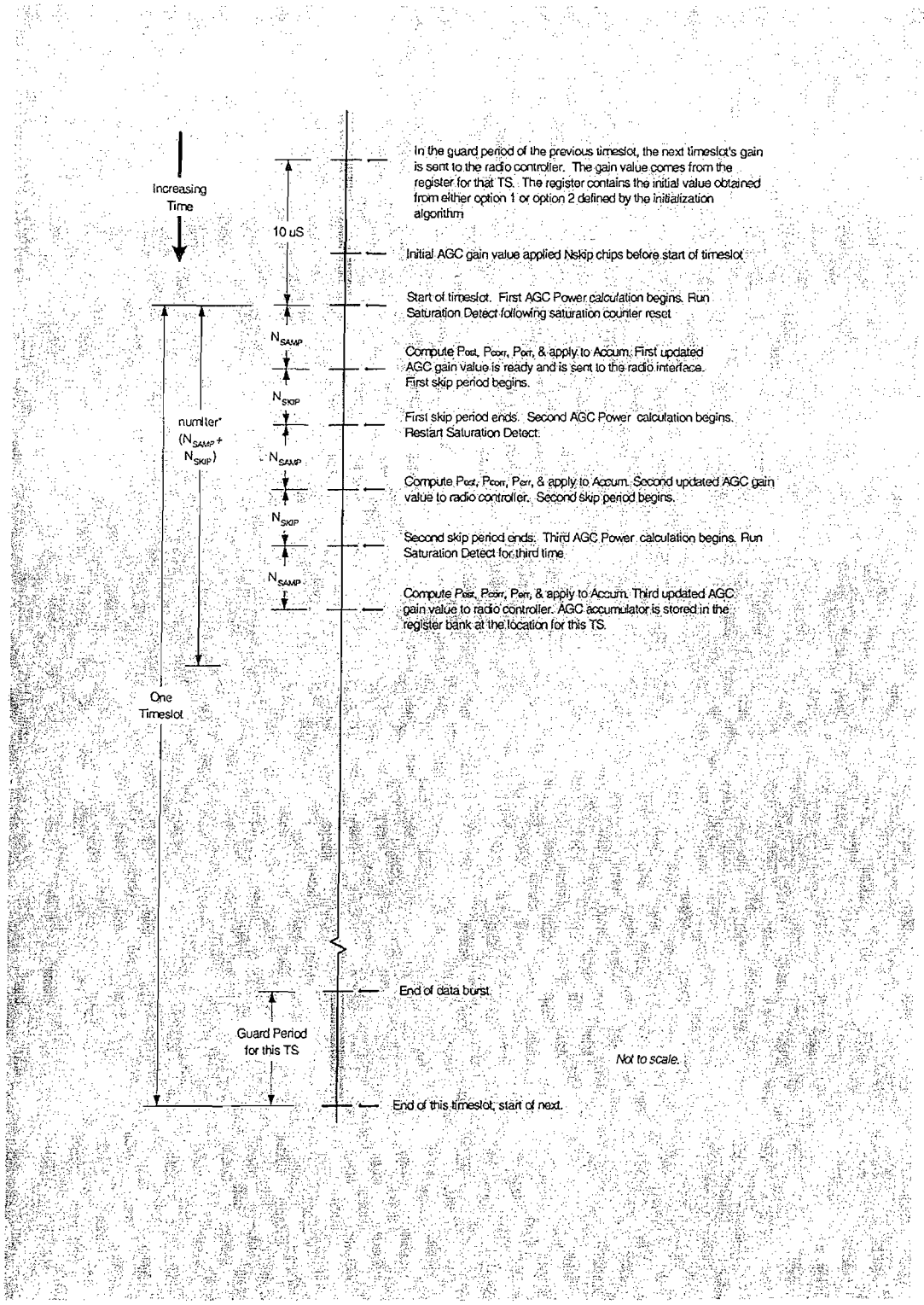

Figure 8: Timeline illustrating the sampling gaps for each iteration

1.1.1.1.4.9.2 Input

- y_{qn} from the ADC

1.1.1.1.4.9.3 Output

- x, a count of the number of saturated samples that occurred within an Nsamp period

1.1.1.1.4.10 Saturation Look Up Table

1.1.1.1.4.10.1 Operation

Based on the number of samples that were saturated during an Nsamp period, a power correction value (P_{corr} in dB) is output from the lookup table. This value is an estimate of and is proportional to the amount of saturation that has occurred. This value is subtracted from the output of the Power Comparator Block, as shown in Figure 1.1.4. The power correction value P_{corr} is based on the same set of samples N_{samp} as the power estimate P_{est}, making the pair fully synchronized. Because the power estimates are in logarithmic form, they allow for a smaller word size of the contents of the Saturation Look Up Table.

The saturation compensation may be bypassed if it is not necessary. Whether it is bypassed or not is based on the configuration parameter, Satcomp_enable, stored in persistent memory (e.g. FLASH ROM). When it is bypassed the output of the Saturation Lookup Table is forced to zero.

The Saturation Look Up Table is required to provide a six-bit output as a function of the saturation counter. The range of the output is 0 to 20 dB in steps of 1 dB, and the input range is 0 to Nsamp, which ranges from a minimum of 40 to a maximum of 320.

The LUT has length equal to Nsamp. Its contents are TBD.

1.1.1.1.4.10.2 Input

- x, from the Saturation Sample Counters and (Positive and Negative) Comparators

1.1.1.1.4.10.3 Output

- P_{corr}, the correction for the power-estimate

1.1.1.1.4.11 Short FIFO and Eraser

1.1.1.1.4.11.1 Operation

The decision to erase data samples, i.e., I and Q set to zero, is based on the sample saturation count x. When x exceeds ζ, the samples are erased in the corresponding Nsamp and Nskip period for a given Loop Iteration. The Short FIFO is necessary because it takes Nsamp samples before a decision can be made, while the number of saturated samples is being counted during the Nsamp period. The size of the Short FIFO is 128 complex samples which is the next largest size in powers of 2 above the default delay required (Nsamp = 80, next largest power of 2 is 128).

The Erase function may be bypassed if it is not necessary. In bypass mode it shall introduce a minimal amount of delay, by bypassing the Short FIFO. Whether it is bypassed or not is based on the configuration parameter, Erase_enable, stored in persistent memory (e.g. FLASH ROM).

1.1.1.1.4.11.2 Input

- y_{qn} from the ADC

1.1.1.1.4.11.3 Output

- To RRC Filter

1.1.1.1.4.12 Gain γ and Bit Selector

1.1.1.1.4.12.1 Operation

The gain γ is used to finely adjust the level of the signal before the Bit Selector. The range for γ is 0.5 to 1, in steps of 0.0625. The gain is applied to the I and Q paths. The parameter γ is stored in persistent memory (e.g. FLASH ROM) as a fixed configuration parameter.

The bit selector selects 6 out of the 9 bits. The selection is based on the parameter Bitselect. The range for Bitselect is from 1 to 3, where 1 represents the action that the uppermost six bits are to be selected, and 2 represents the upper-middle, and 3 represents the lower-middle respectively. The parameter Bitselect is stored in persistent memory (e.g. FLASH ROM) as a fixed configuration parameter.

If the upper most 6 bits are to be selected, then no additional processing is required. If the upper-middle or lower-middle 6 bits are selected, then overflow protection must be performed. This is done for any incoming samples that fall outside the range that can be expressed by the chosen six bits. These extreme sample values are then set to the corresponding maximum positive (e.g. 0x1F) or negative value (e.g. 0x00) that can be expressed in 6-bit two's complement representation. The signal is clipped to a 6-bit maximum positive or negative value through this operation, thus preventing two's complement overflow.

1.1.1.1.4.12.2 Input

- From RRC filter

1.1.1.1.4.12.3 Output

- To Group Delay EQ

1.1.1.1.4.13 Group Delay EQ

1.1.1.1.4.13.1 Operation

The Group Delay EQ compensates for the undesirable group delay variation that is introduced externally by the baseband portions of the RF chipset. The high pass filters in the RF chipset cause this variation in that circuitry. There is one EQ instance for the I path, and one for the Q path.

The Group Delay EQ may be bypassed if it is not necessary. In bypass mode it shall introduce a minimal amount of delay. Whether it is bypassed or not is based on the configuration parameter, EQ_enable, stored in persistent memory (e.g. FLASH ROM). The Group Delay EQ coefficients are stored in persistent memory.

1.1.1.1.4.13.2 Input

- From Bit Selector

1.1.1.1.4.13.3 Output

- To DC Offset Estimator and Canceller

1.1.1.1.4.14 DC Offset Estimator and Canceller

1.1.1.1.4.14.1 Operation

After skipping over the first m samples, the DC Offset Estimator sums up the n sample values and divides them by n, where n is the number of samples that were summed. This is the DC Offset Estimate, which is then subtracted from the output of the Timeslot FIFO (which is known as the RX Sample Buffer in L1 implementation). Note that whenever a value is read out from the Timeslot FIFO, the DC Offset Estimate must be subtracted from it. The value for m is 128, and the value for n is equal to n_{data1}-m, where n_{data1} is the number of samples contained in the data1 field of the timeslot. The offset estimation and cancellation are performed in the I and Q paths independently.

The DC Offset Estimator may be bypassed if it is not necessary. In bypass mode it shall introduce a minimal amount of delay. Whether it is bypassed or not is based on the configuration parameter, DCoffset_enable, stored in persistent memory (e.g. FLASH ROM).

1.1.1.1.4.14.2 Input

- From Group Delay EQ

1.1.1.1.4.14.3 Output

- agcSampOut

1.1.1.1.5 Open Issues

- None at this time